

What is claimed is:

Claims:

- 1 1. A vertical semiconductor device structure, comprising:
2 a substrate defining a substantially horizontal plane;
3 a gate electrode projecting vertically from said substrate and including a
4 vertical sidewall;
5 a spacer flanking said vertical sidewall;
6 a semiconducting nanotube positioned between said gate electrode and said
7 spacer and extending between opposite first and second ends with a substantially
8 vertical orientation;
9 a gate dielectric disposed on said vertical sidewall between said nanotube and
10 said gate electrode;
11 a source electrically coupled with said first end of said nanotube; and
12 a drain electrically coupled with said second end of said nanotube.

- 1 2. The semiconductor device structure of claim 1 wherein said source comprises
2 a catalyst material effective for synthesizing said semiconducting nanotube by a
3 chemical vapor deposition process.

- 1 3. The semiconductor device structure of claim 1 wherein said drain comprises a
2 catalyst material effective for synthesizing said semiconducting nanotube by a
3 chemical vapor deposition process.

- 1 4. The semiconductor device structure of claim 1 wherein said spacer is
2 separated from said substrate by a gap, said gap being filled by an insulating material
3 after said semiconducting nanotube is formed.

- 1 5. The semiconducting device structure of claim 1 wherein said semiconducting
2 nanotube is composed of arranged carbon atoms.

- 1 6. The semiconducting device structure of claim 1 wherein said spacer is
2 separated from said vertical sidewall by a passage.
- 1 7. The semiconducting device structure of claim 6 wherein said passage has
2 horizontal dimensions appropriate for the growth of said semiconducting nanotube
3 and a vertical dimension greater than or equal to a vertical height of said vertical
4 sidewall of said gate electrode.
- 1 8. The semiconducting device structure of claim 6 wherein said passage has a
2 rectangular cross-sectional profile when viewed in a vertical direction.
- 1 9. The semiconducting device structure of claim 6 wherein said source is
2 composed of a catalyst material effective for synthesizing said semiconducting
3 nanotube by a chemical vapor deposition process, said source positioned on said
4 substrate in vertical alignment with said passage.
- 1 10. The semiconducting device structure of claim 9 wherein said spacer is
2 vertically spaced relative to said substrate to define a gap effective for providing a
3 reactant to said catalyst material of said source effective to grow said semiconducting
4 nanotube by a chemical vapor deposition process.
- 1 11. The semiconducting device structure of claim 10 wherein said gap is filled by
2 an insulating material after said semiconducting nanotube is grown by a chemical
3 vapor deposition process.
- 1 12. The semiconducting device structure of claim 6 further comprising a plurality
2 of semiconducting nanotubes positioned horizontally between said gate electrode and
3 said spacer, each of said plurality of semiconducting nanotubes extending vertically in
4 said passage between opposite first and second ends.

1 13. The semiconducting device structure of claim 12 wherein space within said
2 passage not occupied by said plurality of semiconducting nanotubes is filled by an
3 insulating material.

1 14. The semiconducting device structure of claim 1 further comprising a plurality
2 of semiconducting nanotubes positioned horizontally between said gate electrode and
3 said spacer, each of said plurality of semiconducting nanotubes extending vertically
4 between opposite first and second ends.

1 15. The semiconducting device structure of claim 14 wherein at least one of said
2 plurality of semiconducting nanotubes has said first end electrically coupled with said
3 source and said second end electrically coupled with said drain.

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- 1 16. A method of forming a semiconductor device structure, comprising:
2 forming a catalyst pad on a substrate;
3 forming a gate electrode adjacent to the catalyst pad;
4 forming a first spacer on a vertical sidewall of the gate electrode at a position
5 overlying the catalyst pad;
6 forming a second spacer on the first spacer;
7 removing the first spacer to define a passage bounded between the second
8 spacer and the gate electrode in which the passage has an open mouth at one end and
9 the catalyst pad situated at the opposite end;
10 forming a gate dielectric on the vertical sidewall; and
11 synthesizing a semiconducting nanotube on the catalyst pad that extends
12 substantially vertically from the catalyst pad to a free end proximate the open mouth
13 of the passage.
- 1 17. The method of claim 16 wherein removing the first spacer comprises:
2 selectively etching the first spacer relative to the gate electrode, the second
3 spacer, and the substrate.
- 1 18. The method of claim 17 wherein selectively etching the first spacer further
2 comprises:
3 isotropically etching the first spacer.
- 1 19. The method of claim 16 wherein forming the second spacer further comprises:
2 anisotropically etching the second spacer.
- 1 20. The method of claim 16 wherein forming the gate dielectric further comprises:
2 oxidizing the sidewall of the gate electrode to form the gate dielectric.

1 21. The method of claim 16 wherein the first spacer is separated vertically from
2 the substrate by a gap providing a flow path to the catalyst pad, and synthesizing the
3 semiconducting nanotube comprises:

4 directing a reactant through the flow path defined by the gap capable of
5 chemically reacting at the catalyst pad for synthesizing the semiconducting nanotube.

1 22. The method of claim 21 wherein the reactant is a carbonaceous reactant and
2 the semiconducting nanotube is a carbon nanotube.

1 23. The method of claim 21 further comprising:
2 filling the gap with an insulating material after synthesizing the
3 semiconducting nanotube.

1 24. The method of claim 16 further comprising:
2 covering the open mouth of the passage and the gate electrode with a layer of
3 insulating material; and
4 forming a contact in the layer of insulating material electrically coupled with
5 the free end of the semiconducting nanotube.

1 25. The method of claim 16 wherein synthesizing the semiconducting nanotube
2 further comprises:
3 exposing the catalyst pad to a reactant under conditions effective to grow the
4 semiconducting nanotube.

1 26. The method of claim 25 wherein the first spacer is separated from the substrate
2 by a gap providing a flow path to the catalyst pad, and synthesizing the
3 semiconducting nanotube comprises:
4 directing the reactant through the gap to chemically react at the catalyst pad for
5 synthesizing the semiconducting nanotube.

1 27. The method of claim 21 wherein the reactant is a carbonaceous reactant and
2 the semiconducting nanotube is a carbon nanotube.

1 28. The method of claim 16 further comprising:
2 forming a third spacer overlapping a covered portion of the catalyst pad and
3 exposing an uncovered portion of the catalyst pad after forming the gate electrode and
4 the catalyst pad; and
5 removing the uncovered portion of the catalyst pad for reducing a surface area
6 of the catalyst pad.

1 29. The method of claim 28 wherein removing the exposed portion of the catalyst
2 pad comprises:
3 selectively etching the uncovered portion of the catalyst pad relative to the gate
4 electrode and the substrate.

1 30. The method of claim 16 further comprising:
2 forming a contact electrically coupled with the free end of the semiconducting
3 nanotube.

1 31. The method of claim 30 wherein the free end of the semiconducting nanotube
2 projects into a metal plug constituting the contact.

1 32. The method of claim 16 wherein the semiconducting nanotube is a carbon
2 nanotube composed of arranged carbon atoms.

1 33. The method of claim 16 wherein the gate dielectric is formed without
2 adversely affecting the ability of the catalyst pad to catalyze growth of the
3 semiconducting nanotube.

1 34. The method of claim 16 wherein the semiconducting nanotube defines a
2 channel region of a field effect transistor having a channel along which current flow is
3 regulated by application of a control voltage to the gate electrode.

1 35. The method of claim 16 further comprising:
2 synthesizing a plurality of semiconducting nanotubes positioned between the
3 gate electrode and the spacer, each of said plurality of semiconducting nanotubes
4 extending from the catalyst pad to a free end proximate the open mouth of the
5 passage.

1 36. The method of claim 35 further comprising:
2 covering the open mouth of the passage and the gate electrode with a layer of
3 insulating material; and
4 forming a contact in the layer of insulating material electrically coupled with
5 the free end of at least one of the plurality of semiconducting nanotubes.

1 37. The method of claim 36 wherein the plurality of semiconducting nanotubes are
2 carbon nanotubes.

1 38. The method of claim 16 wherein the passage has horizontal dimensions
2 appropriate for the growth of the semiconducting nanotube and a vertical dimension
3 greater than or equal to a vertical height of the vertical sidewall of the gate electrode.

1 39. The method of claim 38 wherein the passage has a rectangular cross-sectional
2 profile when viewed in a vertical direction.

1 40. The method of claim 38 wherein the catalyst pad is positioned on the substrate
2 in vertical alignment with the passage.

- 1 41. The method of claim 40 wherein the spacer is vertically spaced relative to the
- 2 substrate to define a gap effective for providing a reactant to the catalyst pad effective
- 3 to grow the semiconducting nanotube by a chemical vapor deposition process.